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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,120	03/26/2004	Vladislav Potanin	50019.274US01/P05781	8024

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,120	POTANIN ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,15,16 and 18-20* is/are rejected.

7)☒ Claim(s) *10-14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the recitation of "the resistor circuit" in lines 8-9 lacks proper antecedent basis.

In claim 3, the recitation of "the first amplifier" in line 2 lacks proper antecedent basis.

Claims 2 and 4-5 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-9, 15-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Darzy (USP 6,456,051).

Figure 4 shows a circuit providing a detection signal (output of amplifier 28) when a current (current flow through sense resistors Rs) that is delivered to a load (12) decreases below a predetermined threshold voltage comprising coupling current (current passing through transistor 2) to a common node (output node of the filter) through a pass circuit (2) that is

responsive to a first control signal (output of the circuit 22) such that the current is controlled, coupling the current from the common node through a sense circuit (Rs) to the load at an output node (Vo), setting a trip point level with a first resistor circuit (R1) and a first current source (8), the first source is series coupled to the common node through the first resistor circuit, the first current source is configured to provide an approximately constant current level, monitoring a voltage associated with the load to provide a sensed output voltage (output voltage of the sensed resistor), comparing the trip level with the sensed output voltage (28), and asserting the trip point detection signal when the current decreases from a current limit level to a predetermined threshold level as indicated by the change in the sensed output voltage relative to the trip point level as called for in claim 1.

Regarding claim 2, coupling a first input of an amplifier (30) to the output node via the resistor 32, a coupled a second input of the amplifier to the first resistor circuit and the first current source (Vref), providing the first control signal (output of the circuit 22) in response to an output of the amplifier.

Regarding claim 5, the offset is seen as the Voff in figure 4.

Regarding claim 6, figure 4 shows a first current source (80, a first resistor circuit (R1) has an associated tap point (VMD), a pass circuit (2), a sense circuit (Rs), a comparator circuit (28).

Regarding claim 7, the comparator 28 is a low offset comparator.

Regarding claim 8, figure 4 shows an amplifier (30) includes a first input that is coupled to an output node Vo via resistor 32, a second input that is coupled to the first resistor circuit at

Vref, wherein the first control signal (output of the circuit 22) is responsive to an output of the amplifier.

Regarding claim 9, figure 4 shows a second resistor circuit (32), a second current source (34) is coupled to the output node through the second resistor circuit.

Regarding claim 15, figure 4 shows a first voltage drop means (resistor 26), a pass means (2), a sense means (Rs), a comparator means (28).

Regarding claim 16, figure 4 shows a curent source means (8), a resistor means (26).

Regarding claim 18, figure 4 shows sense means a resistor Rs.

Regarding clam 19, pass means is a FET.

Regarding claim 20, the comparator 28 is a low offset comparator.

5. Claims 15-16, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 5-336679.

Figure 1 shows a first voltage drop means (resistor R3, R4) that is coupled to a common node (collector of transistor Q1) and arranged to provide a trip point level at a tap point, a pass means (Q1) is coupled in between the common node and the input source node, a sense means (R2) that is coupled between the common mode and an output node, a comparator means (8) includes a first input that is coupled to the tap point, a second input that is coupled to the output node, wherein the comparator means is arranged to assert the trip point detection signal when the curent decreases from a current limit level to a predetermined threshold level as called for in claims 15 and 18.

Regarding claim 16, figure 3 shows a constant current source (R23), a resistor means (R22).

Regarding claim 20, the comparator 8 is a low offset comparator.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP 5-336679. Figure 1 shows a first voltage drop means (resistor R3, R4) that is coupled to a common node (collector of transistor Q1) and arranged to provide a trip point level at a tap point, a pass means (Q1) is coupled in between the common node and the input source node, a sense means (R2) that is coupled between the common node and an output node, a comparator means (8) includes a first input that is coupled to the tap point, a second input that is coupled to the output node, wherein the comparator means is arranged to assert the trip point detection signal when the curent decreases from a current limit level to a predetermined threshold level.

Figure 1 of JP 5-336679 shows a bipolar transistor as a pass means instead of a field effect transistor as called for in claim 19. However, it is known in the art that field effect transistor consumes less power and occupies less space on a chip than a bipolar transistor. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to replace a bipolar transistor with a field effect transistor for the purpose of saving space.

Allowable Subject Matter

8. Claims 3-4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. Claims 10-14 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

5/10/2005